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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,629	04/01/2004	Philippe Bienvenu	03-RO-111; B5921US; 2269-	2835

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EXAMINER	
RUTLAND WALLIS, MICHAEL	
ART UNIT	**PAPER NUMBER**
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

A.1

Office Action Summary	Application No.	Applicant(s)	
	10/817,629	BIENVENU ET AL.	
	Examiner	Art Unit	
	Michael Rutland-Wallis	2835	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/01/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *See Continuation Sheet*.

Continuation of Attachment(s) 6). Other: English Translation of DE 19928 760.

DETAILED ACTION

35 USC § 112 6th Notification

Applicants recitation of "a first means for" and "a second means for" in claims 1-8, are treated to evoke 112 sixth paragraph, Applicants are hereby notified said claims will be treated accordingly in this Office action. MPEP 2181 [R-5] I.

Claim Rejections - 35 USC § 112

Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has failed to set forth in the disclosure an adequate disclosure showing what is meant by the second means for, in claim 1. Therefore claim 1 fails to comply with 112 2nd paragraph to particularly point out and distinctly claim the invention. See MPEP 2181 [R-5] II.

Claim Objections

Claim 2 is objected to as "said delay" is unclear. Claim 1 refers to two different delay times. Applicants should amend said limitations in at least claim 2 to clearly claim which delay Applicant intends in claim 2.

Claim 3 is objected to as "maximum expected duration" it is unclear the meets and bounds of said limitation.

Claim 11 is objected to "a second disabling" is unclear. Applicant has not recited a first disabling.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 3-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Pechlaner et al. (DE 199 28 760 A1) see English translation attached to this action.

With respect to claims 1 Pechlaner teaches a device for protecting a circuit against a polarity reversal (Fig. 1) of a connection to a DC power supply (not shown see supply terminals Vbb), comprising: a controllable switch (item 5 smart power switch) interposed on said connection between a first terminal (Vbb) of a first voltage of said DC power supply and a first terminal (see terminal 2) of said circuit; and first means (formed with capacitor item 9 connected to item 6 further see page 5 lines 15-20 to effect the switching of item 3 via controller 4) for turning-off with a delay the switch in the presence of a reverse polarity; and second means (formed by delay associated with the

transmit of a control signal from the controller to the switch) for turning on the switch (5) with a delay shorter than the turn-off delay, when the polarity is normal.

With respect to claim 3 Pechlaner teaches the first terminal of the circuit to be protected is a ground connection terminal (item 2 connected to chassis of the system)

With respect to claim 4 Pechlaner teaches the first means comprise a microcontroller (item 4 "controller") having an output controlling, directly or via a selective delay element, said switch

With respect to claim 5 Pechlaner teaches the switch is a MOS transistor with an N channel (see schematic symbol in Fig. 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pechlaner et al. (DE 199 28 760 A1)

With respect to claim 2 Pechlaner teaches delay is chosen such that an inductive load is switched by the controllable switch (item 5) and not other means (such as item 6) see page 5 lines 15-20. Pechlaner does not teach the delay is chosen based on transient polarity reversal, however the capacitor of Pechlaner would provide a

protection from transient reversals via the time constant associated with the capacitor item 9. It would have been obvious to one of ordinary skill in the art at the time of the invention to size the capacitor appropriately to provide a longer or shorter delay based on expected transients from the load or supply in order to insure the load is switched by the controllable switch to prevent damage.

With respect to claim 6 Pechlaner is silent on the circuitry contained within the first means however output terminals of controllers are typically formed with resistive connections. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a resistor in the connection line from the controller to the switch in order to regulate the voltage drop supplied to protect the switch from damage.

With respect to claim 7 Pechlaner is silent on the use of the first or second resistor Pechlaner teaches the connection of a control diode (item 13) in the controller, however is silent on the nature of the detailed connection of the diode in relation to the control circuitry contained within the controller. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a series of resistors in the connection line from the controller to the switch in order to regulate the voltage drop supplied to protect the switch from damage.

With respect to claim 8 Pechlaner teaches the connection of a control diode (item 13) in the controller, however is silent on the nature of the detailed connection of the diode in relation to the control circuitry contained within the controller. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the zener diode as the control diodes are commonly used as control diodes.

Claims 9-10 and 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pechlaner et al. (DE 199 28 760 A1) in view of Yoshida (U.S. Pat. No. 5,726,505)

With respect to claims 9-10 and 13-20 Pechlaner teaches a circuit (Fig. 1), comprising: a switch (3) operable to conduct a current to a first node of a power supply (connected at terminal Vbb) when the first node has a predetermined polarity relative to a second node of the power supply; and a first delay (formed by delay associated with the transmit of a control signal from the controller item 4 to the switch item 3) coupled to the switch and operable to disable the switch from conducting current. Pechlaner is silent on teaching the disabling of the switch from the conducting current is preformed at a predetermined time after the polarity reverses in part because a circuitry within the controller is not described or shown in detail. Yoshida teaches system similar protection system (Fig. 2) wherein Yoshida teaches a detection and control circuit (item 6) to operate with delay determined by the component value of the circuitry contained within the circuit. It would have been obvious to one of ordinary skill in the art at the time of the invention to include a predetermined delay if in fact the delay present in Pechlaner is not predetermined in order to allow sufficient time to determine polarity before closing the switch to better protect the load.

With respect to claim 11 Pechlaner teaches a second delay disabling the switch in response to a normal condition of the current (when the removal of power occurs in device of Pechlaner capacitor item 9 provides a delay).

With respect to claim 12 Pechlaner teaches the switch comprises a transistor (see schematic symbol in Fig. 1); and the first delay (4) is operable to discharge the gate capacitance (gate capacitance is inherent to MOSFETs) of the transistor.

Conclusion

The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure. Makaran (U.S. Pat. No. 6,611,410) teaches a similar system to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MRW

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

PTO 07-1015

German Laid-Open Patent Application

Document No. DE 199 28 760

POLARITY PROTECTION FOR AT LEAST ONE INTELLIGENT SEMICONDUCTOR SWITCH

[Verpolschutz fuer mindestens einen intelligenten Halbleitschalter]

Pechlaner, Andreas et al.

UNITED STATES PATENT AND TRADEMARK OFFICE

Washington, D.C. November 2006

Translated by: Schreiber Translations, Inc.

Country	:	Germany
Document No.	:	DE 199 28 760 A1
Document Type	:	Laid-Open Patent Application
Language	:	German
Inventor	:	Pechlaner, Andreas et al.
Applicant	:	Siemens AG
IPC	:	H 02 H 3/18
Application Date	:	06.23.1999
Publication Date	:	01.04.2001
Foreign Language Title :		Verpolschutz fuer mindestens einen intelligenten Halbleitschalter
English Title :		Polarity Protection for at Least One Intelligent Semiconductor Switch

(Please note, footnote should be inserted from Toolbar Menu) /1[1]

Polarity protection for at least one intelligent semiconductor switch is provided, which is connected at the output side to a chassis-connected load during normal operation. The intelligent semiconductor switch is connected during normal operation to a reference potential terminal for logical circuitry via another oppositely connected semiconductor switch. With this arrangement, there is only a small voltage drop during normal operation between the reference potential terminal of the intelligent semiconductor switch and the actual reference potential. In the event that the polarity is wrong, thermal damage to the intelligent semiconductor switch is prevented.

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Description

The invention relates to polarity protection of at least one intelligent semiconductor switch, which is connected to a chassis connected load during normal operation.

Intelligent semiconductor switches or so called smart power switches, are known in the state of the art under the name PROFET. A principle arrangement of such semiconductor switch is described, e.g., in Siemens Data Sheets "smart power switches", Data Sheets 04.97, p. 506 and further. In addition to the semiconductor switch proper, which is connected on the drain side to a high power supply potential and on the source side to a chassis connected load, the smart power switch has a number of functions, which protect the semiconductor switch against damage. Thus, it has, e.g., current limiting, overvoltage protection limiting, as well as a temperature sensor. The smart power switch described above is made as a high-side semiconductor switch. For that purpose, it has a charge pump, which must raise the voltage at its gate electrode above the

[1] Numbers in the margin indicate pagination in the foreign text.

voltage at its source electrode in order to be able to hold the semiconductor switch in the conducting state. The smart power switch also has an input, to which a control signal can be applied. A controller can receive an appropriate fault signal in case of a fault condition through a status output ST. Logical circuits of the smart power switch are also connected to a reference potential GND, which is normally isolated from the chassis connection for the external load.

The above-described intelligent semiconductor switch is used in many electronic circuits such as, for instance, in motorized vehicles. The wrong polarity is basically a problem for power supply connections as well as for both the logical circuits and for the power semiconductor switches. In the event that the polarity of an intelligent semiconductor switch is wrong, a higher current flows through the reference potential connection of the logical switching circuits. Without a special protection, the high current would normally result in damage to the intelligent semiconductor switch. This is because of high loss power in the logical circuits.

It us also known from the state of the art to provide an external resistor between the reference potential terminal of the logical circuit and the reference potential. In the event of the wrong polarity, the voltage goes to the external resistor, so the major part of the loss power occurs outside the intelligent semiconductor switch. The provision of such resistor, which is also referred to as the ground resistor, results in a serious disadvantages. During normal operation, the voltage applied to the control electrode of the semiconductor switch should be higher enough than the cutoff voltage of the semiconductor switch. If the above-described resistor is provided, a voltage drop across the resistor will clearly reduce the effective control voltage. This can result in undesired opening if the intelligent semiconductor switch when the voltage applied to the control input, which is generated by a microcontroller, goes down.

In addition to the loss power generated at the external resistor in the event of the wrong polarity, substantial loss power is generated in the process specific reverse biased diodes of the power semiconductor switch in the smart power switch.

In order to eliminate the disadvantage related to the external resistor, US 4,857,985 teaches a semiconductor switch replacing the resistor, the switch being provided between the logical circuit device and the reference potential. The semiconductor switch is switched in such a manner that in normal operation it is conducting so that there is only a very small voltage drop across the switch. In the event of the wrong polarity, the semiconductor switch is switched to the blocked state because the voltage at its control electrode is well below the source potential. The integrated reverse biased diode is then switched to the blocked state so as to prevent current from flowing in the logical circuits. The control electrode of the semiconductor switch is connected for that purpose during normal operation to a higher power supply potential V_{bb}. The device disclosed in US 4,857,985 has, however, a disadvantage because no inductive load can be driven by the logical circuit device 10. If the power supply voltage increases during normal operation, the inductive load cannot be switched because of the sudden blocking of the semiconductor switch. This would result in high overvoltage in the logical circuitry, which can cause damage to the circuitry.

It is, therefore, an object of the invention to provide a switching device, which is protected against the wrong polarity and also has sufficient protection in the event the inductive load is used.

This object is accomplished by using the distinguishing features defined in claim 1.

According to the invention, in an intelligent semiconductor switch of the above type, the reference potential terminal for logical circuitry in normal operation is connected, via another oppositely connected semiconductor switch with a lower reference

potential, with the control electrode of the additional semiconductor switch being connected to the reference potential terminal of the logical circuitry via a storage capacitor.

With this arrangement, there is only a small voltage drop across the protection circuit during normal operation. At the same time, A constantly high control voltage is guaranteed for the power semiconductor switch. Further, the additional semiconductor switch blocks the current flow in the event of the wrong polarity inside its auxiliary reverse biased diode. With this arrangement, there is no loss power generated in the intelligent semiconductor switch in the event of the wrong polarity. In addition, with the switching device according to the invention, there is no problem with the switching of an inductive load in the event of a loss of the positive power supply voltage in normal operation. The storage capacitor, which is connected between the control electrode of the additional semiconductor switch and the reference potential terminal of the logical circuitry is used to maintain the additional semiconductor switch in the conducting state for a time that is long enough for the inductance to switch over during this time. When the storage capacitor has been discharged, the additional semiconductor switch is blocked.

In a preferred embodiment, the control electrode of the additional semiconductor switch is connected to the high power supply potential terminal via a resistor. This resistor is used during normal operation to bring the control electrode of the additional semiconductor switch to a voltage that is high enough to maintain it in the conducting state.

In another preferred embodiment, a plurality of intelligent semiconductor switches have their reference potential terminals that are connected together. The reference potential terminals of all

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Intelligent semiconductor switches are, therefore, connected to the same reference potential. In the event of the wrong

polarity, all the intelligent semiconductor switches are protected at the same time by means of the additional semiconductor switch. According to the invention, the efficient polarity protection is ensured for a plurality of smart power switches using a small number of components.

Other advantageous embodiments are defined in the subservient claims.

The invention will now be described with reference to two accompanying drawings, in which:

Fig. 1 shows polarity protection according to the invention for a single intelligent semiconductor switch, and

Fig. 2 shows polarity protection for two intelligent semiconductor switches.

Fig. 1 shows a simplified representation of an intelligent semiconductor switch having polar protection according to the invention. The smart power switch consists of a semiconductor switch 3, which is made as MOSFET, and a control device 4. The control device 4 has a control input IN on the one hand and is connected to a control terminal of the MOSFET 3. The control device 4 has among other things a charge pump, which brings the gate terminal potential to a level above the potential of the source terminal of the MOSFET 3 in order to switch it over to the conducting state. The MOSFET 3 is connected on its drain side to a power supply potential terminal 1, to which a high power supply potential V_{bb} is applied during normal operation. On the source side, the MOSFET 3 is connected to an inductive load 11, which has the other terminal connected to a chassis potential terminal 2. The source terminal of MOSFET 3 is also an output OUT of the smart power switch 5. The smart power switch 5 also has a reference potential terminal GND. This terminal is connected to a reference potential terminal 12 via an oppositely connected MOSFET 6. The oppositely connected MOSFET means that the source terminal is connected to the reference potential terminal GND, and the drain side of the MOSFET 6 is connected to the reference potential terminal proper 12 of the logical

circuitry. The gate of the MOSFET 6 is connected to a first power supply potential terminal 1 via a resistor 7. It is also helpful to expose the resistor to another voltage such as then power supply voltage V_{bb}. A capacitor 9 is connected between the gate terminal and the source terminal of the MOSFET 6. The capacitor provides a high gate - source capacity, which is used, in the event that the power supply voltage V_{bb} at the semiconductor switch 3 is lost, to maintain the MOSFET 6 for certain time in the conducting state so that the inductive load can complete its switching off from the MOSFET 6 and the control diode 13 of the control device 4. To protect the gate of the MOSFET 6, a Zener diode is connected in a parallel with the capacitor 9, with the anode side thereof connected to the reference terminal GND.

The manner of functioning of the polarity protection according to the invention will now be briefly described.

The semiconductor switch 6 is controlled and become conductive by application of power supply voltage V_{bb} through the resistor 7, which is chosen to be very high. The Zener diode 10 protects the gate of the MOSFET 6 against the high voltage. The breakthrough voltage of the Zener diode 10 should be chosen in such a manner in this case that it has to be below the maximum allowable gate voltage for the MOSFET 6. In the event that the power supply voltage is lost, the capacitor 9 will still hold the MOSFET 6 in the conducting state for short time longer. This facility ensures that the inductive load that is switched over by the smart power switch should not switched off through its path. The MOSFET 6 is sized in such a manner that then voltage drop should be as small as possible in normal operation.

In the event of the wrong polarity, the first power supply potential terminal 1 as well as the second power supply potential terminal 2 and the reference potential terminal 12 block the MOSFET 6 because the gate potential cannot go any higher, as well as its source potential. Because the source terminal of the MOSFET 6 is connected to the reference potential

terminal GND of the smart power switch, the auxiliary reverse biased diode of the MOSFET T1 goes to the blocked state. For this reason, a current flow in the control (logical circuitry) of the smart power switch is prevented. The control device 4 can also have means that controls the MOSFET 3 to go conductive in the event of the wrong polarity in order to limit its loss power.

A state of the art control device for the high-side MOSFET is disclosed, e.g., in EP 0 572 706 A1.

The polarity protection according to the invention can also be used in a simple manner for a plurality of smart power switches. Fig. 2 shows two smart power switches 5, 5'. The are connected together at their reference potential terminals GND, GND'. To protect all parallel-connected smart power switches and their logical circuitries in the event of the wrong polarity, it takes only a single oppositely connected MOSFET 6, which provided between the reference potential terminals GND, GND' and the actual reference potential terminal 12.

The polarity protection device consisting of the MOSFET 6, the resistor 7, the capacitor 9, and the Zener diode 10 can be integrated into a module. It is preferred that the polarity protection device be made as a separate semiconductor chip. It is also possible to integrate the polarity protection device directly in the semiconductor switch 5.

The invention allows for simple polarity protection of an intelligent semiconductor switch, and it also can handle a power supply voltage loss in normal operation, thus providing a better protection for smart power switches.

List of reference numerals:

1 First power supply potential terminal

2 Second power supply potential terminal

3 Semiconductor switch

4 Control device

5 Intelligent semiconductor switch

6 Semiconductor switch

7 Resistor

8 Integrated reverse biased diode

9 Storage capacitor

10 Zener diode

11 Load

12 Reference potential terminal

IN Control input

OUT Output

GND Reference potential terminal

Claims

1. Polarity protection for at least one intelligent semiconductor switch (5), which is connected on the output side to a load (11) connected to the chassis potential in normal operation and is connected, via a reference potential terminal (GND) for logical circuitry (4) in normal operation

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via an additional oppositely connected semiconductor switch (6) to a lower reference potential (12), with the control electrode of the additional semiconductor switch (6) being connected to the reference potential terminal (GND) via a storage capacitor (9).

2. The polarity protection of claim 1, characterized by the fact that the intelligent semiconductor switch (5) has a control device (4), which is controlled according to a control signal at the control input (IN) of the semiconductor switch (3).

3. The polarity protection of claim 1 or 2, characterized by the fact that the control terminal of the additional semiconductor switch (6) is exposed in normal operation to a higher power supply potential (1) via a resistor.

4. The polarity protection of any of claims 1 through 3, characterized by the fact that a Zener diode (10) is connected in parallel with the storage capacitor (9).

5. The polarity protection of any of claims 1 through 4, characterized by the fact that the load (11) is an inductive behavior load.

6. The polarity protection of any of claims 1 through 5, characterized by the fact that a plurality of intelligent semiconductor switches (5, 5') are connected to each other at their respective reference potential terminals (GND, GND').

7. The polarity protection of any of claims 1 through 6, characterized by the fact that the terminal of the load (11) on the chassis side is connected to a lower reference potential terminal (12).

FIG 1

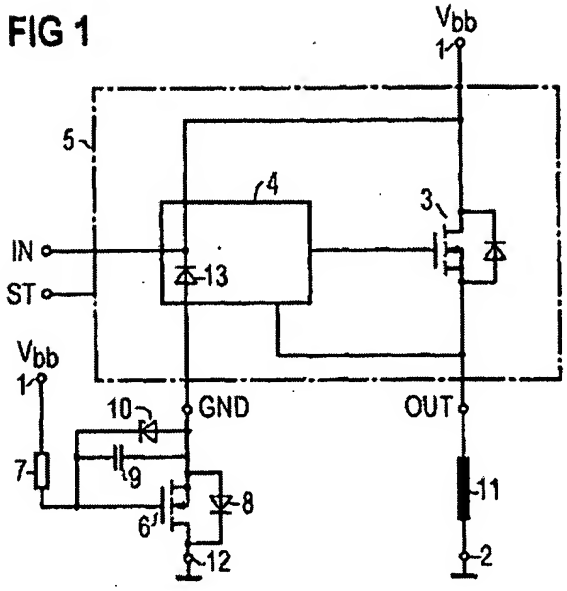
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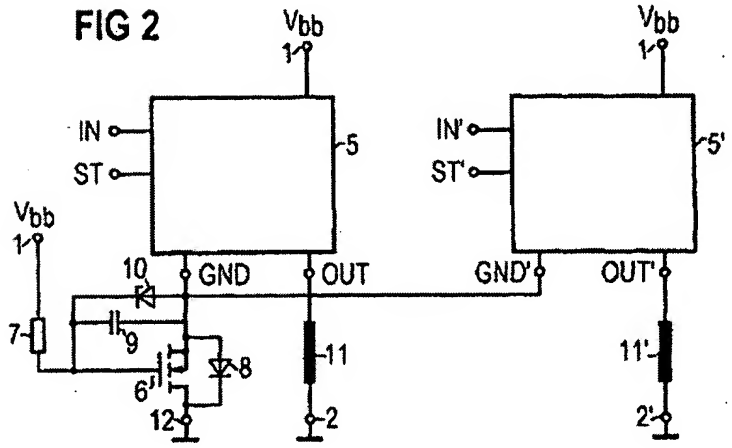
FIG 2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